200G QSFP56 to 2xQSFP56 Breakout Active Optical Cable

Features

- 4x 50Gb/s PAM4 modulation
- Hot pluggable
- SFF-8665 compliant QSFP56 port
- SFF-8636 compliant I2C management
- Single 3.3V power supply
- Max 4.5W power dissipation each end, with retiming
- 0 to 70°C case temperature operating range
- RoHS compliant
- Metal enclosure for low EMI

Applications

- Datacom/Telecom Switch & Router connections
- High speed multi-channel parallel data connections
- High performance computing, server and data storage

Compliance

- 200GBASE-SR4 Ethernet (PAM4)
- Compliant with IEEE 802.3cd

Description：

Active Optical Splitter Cable is used in 200 Gigabit Ethernet links over OM3/OM4/OM5 multi-mode fiber, which provides connectivity between system units with a 200GbE connector on one side and two separate 100GbE connectors on the other two sides. The cable connects data signals from each of the 4 MMF (Multi Mode Fiber) pairs on the single QSFP56 end to the dual pair of each of the QSFP56 multi-port ends.

Active Optical Splitter Cable is compliant with the QSFP-MSA and with 200GBASE-SR4 specification. Digital diagnostics functions are available via the I2C interface as specified by CMIS V4.0. The transceiver is RoHS 2.0 compliant and lead-free per Directive 2011/65/EU.

Absolute Maximum Ratings

Table1-Absolute Maximum Ratings

Parameter	Symbols	Min	Typical	Max	Unit	Notes
Storage Temperature	TSTG	-40	-	+85	ºC	
Operating Temperature	Top	0		70	ºC	
3.3V Supply Voltage	V_{CC3}	-0.5	-	+3.6	V	
Relative Humidity	RH	+5		+85	%	
Distance		1		50	m	

Recommended Operating Conditions

Table2-Recommended Operating Conditions

Parameter	Symbol	Min	Typical	Max	Unit	Notes
Operating Case Temperature	T_C	0	-	+70	℃	
Power Supply Voltage	Vcc	3.14	3.3	3.47	V	
Power dissipation(200G retiming on all lanes)	Pd_{200G}	-	-	4.5	W	1
Power dissipation(100G retiming on all lanes)	Pd_{100G}	-	-	2.5	W	1

Note: 1 Per terminal

Electrical Characteristics

Table3-Electrical Characteristics

Parameter	Symbol	Unit	Min	Typ.	Max	Notes
Transmitter						
Signaling rate(each lane)	SR	GBd	26.5625±100ppm			
Differential data input voltage per lane	Vin,pp,diff	mV	900	-	-	
Differential termination mismatchal	-	%	-	-	10	
Single-ended voltage tolerance range	-	V	-0.4	-	3.3	
DC common mode voltage	-	mV	-350	-	2850	
Receiver						
Single Rate(each lane)	SR	GBd	26.5625±100ppm			

AC Common Mode Voltage	-	mV	-	-	900	

Differential termination mismatch	-	%	-	-	10	
Transition time(min,20% to 80%)	-	ps	9.5	-	-	
DC common mode voltage	-	mV	-350	-	2850	
Error Bit Rate	BER	-	-	-	2.3E-4	Note1

Note: 1 PRBS31Q@26.5625Gbd PAM4

Recommended Interface Circuit

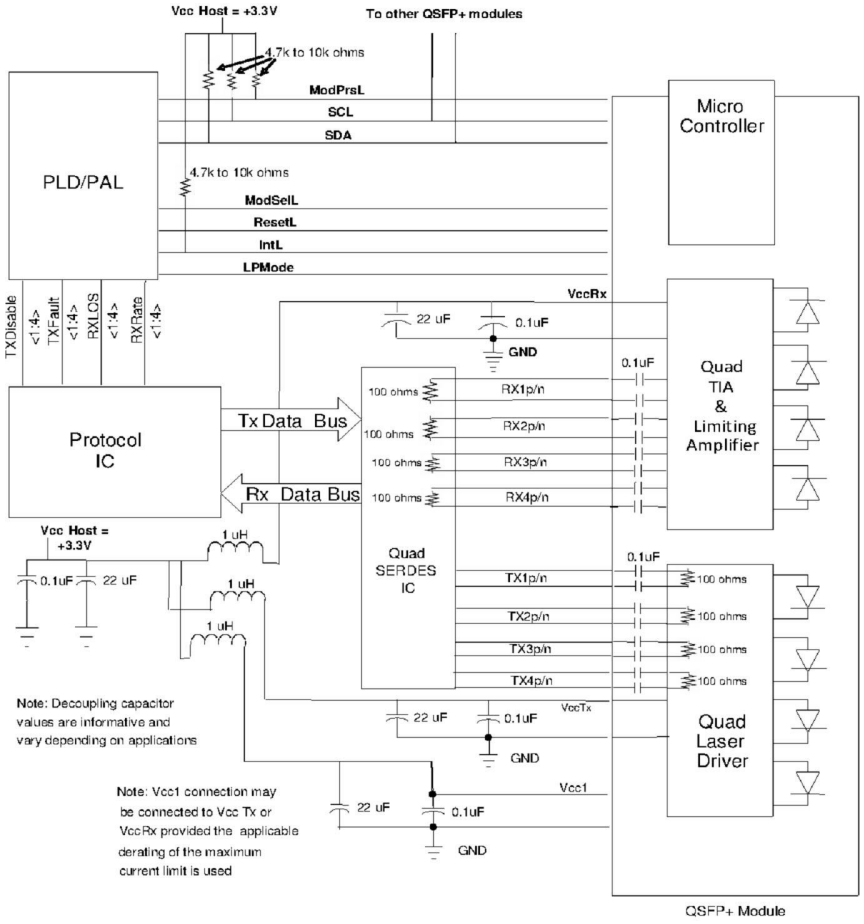


Figure 1—Recommended Interface Circuit

Pin arrangement

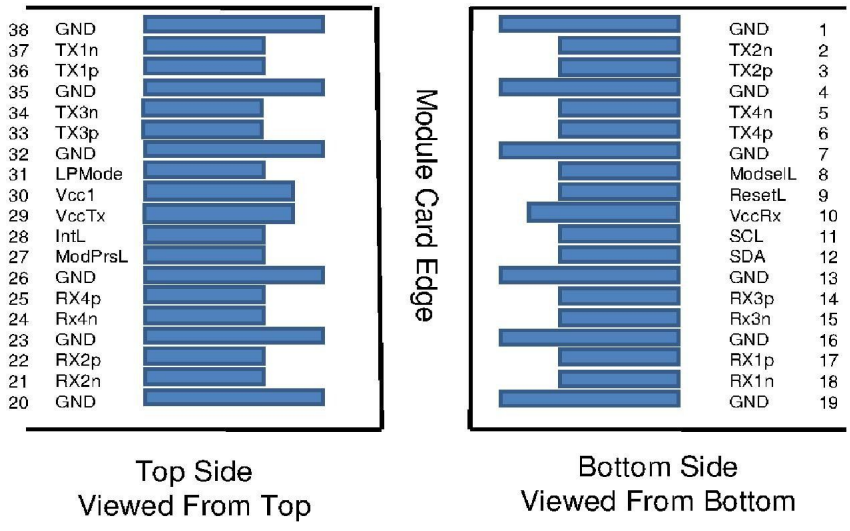


Figure 2—QSFP56 MSA-compliant 38-pin connector

Pin Function Definitions

Table4-Pin Function Definitions

Pin	Symbol	Name/Description	Ref.
1	GND	Ground	1
2	Tx2n	Transmitter Inverted Data Input	
3	Tx2p	Transmitter Non-Inverted Data Input	
4	GND	Ground	1
5	Tx4n	Transmitter Inverted Data Input	
6	Tx4p	Transmitter Non-Inverted Data Input	
7	GND	Ground	1
8	ModSelL	Module Select	
9	ResetL	Module Reset	
10	Vcc Rx	+3.3V Power Supply Receiver	
11	SCL	2-wire serial interface clock	
12	SDA	2-wire serial interface data	
13	GND	Ground	1
14	Rx3p	Receiver Non-Inverted Data Output	
15	Rx3n	Receiver Inverted Data Output	
16	GND	Ground	1
17	Rx1p	Receiver Non-Inverted Data Output	
18	Rx1n	Receiver Inverted Data Output	
19	GND	Ground	1
20	GND	Ground	1
21	Rx2n	Receiver Inverted Data Output	
22	Rx2p	Receiver Non-Inverted Data Output	
23	GND	Ground	1
24	Rx4n	Receiver Inverted Data Output	
25	Rx4p	Receiver Non-Inverted Data Output	
26	GND	Ground	1
27	ModPrsL	Module Present	
28	IntL	Interrupt	
29	VccTx	+3.3V Power supply transmitter	
30	Vcc1	+3.3V Power supply	
31	LPMode	Low Power Mode	
32	GND	Ground	1
33	Tx3p	Transmitter Non-Inverted Data Input	
34	Tx3n	Transmitter Inverted Data Input	
35	GND	Ground	1

36	Tx1p	Transmitter Non-Inverted Data Input	
37	Tx1n	Transmitter Inverted Data Input	
38	GND	Ground	1

Notes：

[1] Circuit ground is internally isolated from chassis ground

Module Block Diagram (200G End)

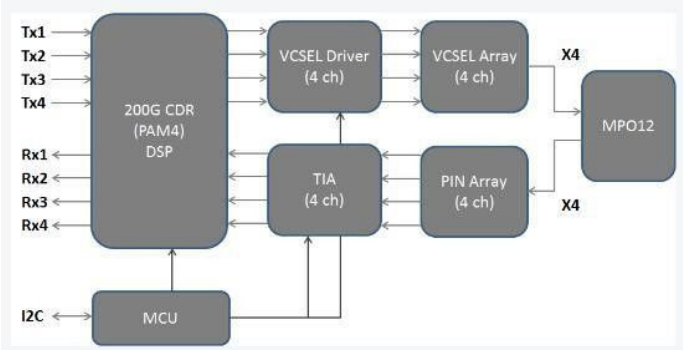


Figure 3—Module Block Diagram (200G End)

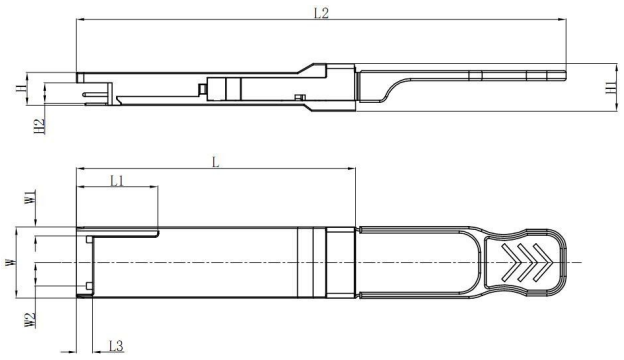
Monitoring Specification

2-Wire Serial Address 1010000x
Lower Page 00h
0 Identifier
1- 2 Status
3- 21 Interrupt Flags
22- 33 Free Side Device Monitors
34- 81 Channel Monitors
82- 85 Reserved
86- 98 Control
99 Reserved
100-104 Hardware Interrupt Pin Masks
105-106 Vendor Specific
107 Reserved
108-110 Free Side Device Properties
111-112 Assigned for use by PCI Express
113 Free Side Device Properties
114-118 Reserved
119-122 Password Change Entry Area (Optional)
123-126 Password Entry Area (Optional)
127 Page Select Byte

Upper Page 00h	Optional Page 01h	Optional Page 02h	Optional Page 03h
128 Identifier	128 CC_APPS	128-255 User EEPROM Data	128-175 Free Side Device Thresholds
129-191 Base ID Fields	129 AST Table Length (TL)		
	130-131 Application Code Entry 0		
	132-133 Application Code Entry 1		
	134-253 other entries		176-223 Channel Thresholds
192-223 Extended ID			224 Tx EQ & Rx Emphasis Magnitude ID
224-255 Vendor Specific ID			225 RX output amplitude indicators
			226-241 Channel Controls
			242-251 Channel Monitor Masks
	254-255 Application Code Entry TL		252-255 Reserved

Figure 4—Memory Ma

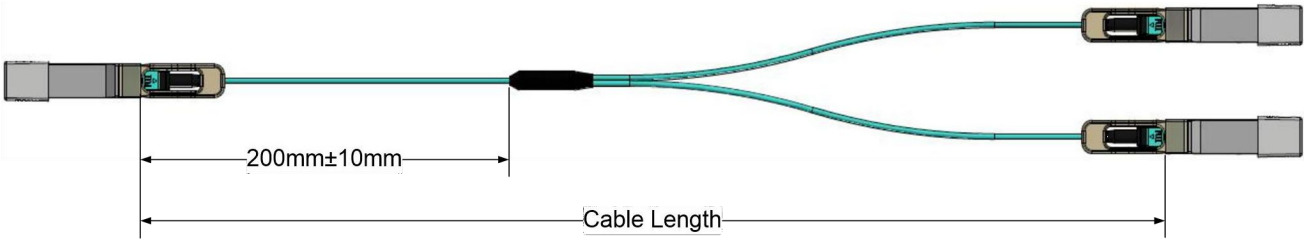
Mechanical



Unit mm

	L	L1	L2	L3	W	W1	W2	H	H1	H2	L	L1	L2	L3
Max	72.2	-	128	4.35	18.45	-	6.2	8.6	12.0	5.35	72.2	-	128	4.35
Type	72.0	-	-	4.20	18.35	-	-	8.5	11.8	5.2	72.0	-	-	4.20
Min	68.8	16.5	124	4.05	18.25	2.2	5.8	8.4	11.6	5.05	68.8	16.5	124	4.05

Figure 5—Mechanical Diagram of Cable



Cable Length

Table5-Cable Length

Parameter	Value	Units
Diameter	3±0.2	mm
Minimum bend radius	30	mm
Length tolerance	1 m ≤length ≤ 4.5 m +15 / -0	cm
	5 m ≤length ≤ 14.5 m +30 / -0	cm
	Length≥15.0 m +2% / -0	m
Cable color	Aqua	

Connectivity Schematic

Table6-Connectivity Schematic

200Gb/s Side	100Gb/s Side
	Port 1
TX1	RX1
RX1	TX1
TX2	RX2
RX2	TX2
	Port 2
TX3	RX1
RX3	TX1
TX4	RX2
RX4	TX2