200G QSFP56 SR4 Transceivers

Features

- Hot-pluggable QSFP form factor
- Compliant to CMIS V4.0
- Maximum link length of 100m on OM4 fiber with KP4 FEC
- +3.3V single power supply
- Power dissipation < 6W
- Operating case temp Commercial: 0°C to +70 °C
- MPO-12 APC connector
- RoHS compliant

Applications

- 200GBASE-SR4 Ethernet

General Description

This product is a parallel 200Gb/s Quad Small Form Factor Pluggable (QSFP56) optical module. It provides increased port density and total system cost savings. The design is compliant to IEEE802.3bs Annex120E (200GAUI-4 C2M). The QSFP56 full-duplex optical module offers 4 independent transmit and receive channels, each capable of 53.125Gb/s operation for an aggregate data rate of 200Gb/s on 70 meters of OM3 multi-mode fiber.

An optical fiber cable with an MTP/MPO-12 APC connector can be plugged into the QSFP56 SR4 module receptacle. Proper alignment is ensured by the guide pins inside the receptacle. The cable usually cannot be twisted for proper channel to channel alignment. Electrical connection is achieved through a QSFP56 MSA-compliant edge type connector.

The central wavelengths of all the 4 parallel lanes are 850nm. It contains an optical MPO-12 APC connector for the optical interface and a 38-pin connector for the electrical interface. Host FEC is required to support up to 70m OM3 multi-mode fiber transmission.

The product is designed with form factor, optical/electrical connection and digital diagnostic interface according to the QSFP56 Multi-Source Agreement (MSA). It has been designed to meet the harshest external operating conditions including temperature, humidity and EMI interference.

Functional Description

The module incorporates 4 parallel channels, on 850nm Center Wavelength, operating at 50G per channel. The transmitter path incorporates a 4-channel CDR retimer, a quad channel VCSEL drivers together with a VCSEL array. On the receiver path, a photo diode array optics are coupled with an 4- channel CDR retimer. The electrical interface is compliant with IEEE 802.3bs and QSFP56 MSA in the transmitting and receiving directions, and the optical interface is compliant to QSFP56 MSA with MPO-12 APC Optical Connector. Figure 1 shows the functional block diagram of this product.

A single +3.3V power supply is required to power up this product. All the power supply pins are internally connected and should be applied concurrently. As per MSA specifications the module offers seven low speed hardware control pins (including the 2-wire serial interface): ModSelL, SCL, SDA, ResetL, InitMode, ModPrsL and IntL.

Module Select (ModSelL) is an input pin. When held low by the host, this product responds to 2-wire serial communication commands. The ModSelL allows the use of this product on a single 2-wire interface bus – individual ModSelL lines must be used.

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Serial Clock (SCL) and Serial Data (SDA) are required for the 2-wire serial bus communication interface and enable the host to access the memory map.

The ResetL pin enables a complete reset, returning the settings to their default state, when a low level on the ResetL pin is held for longer than the minimum pulse length. During the execution of a reset the host shall disregard all status bits until it indicates a completion of the reset interrupt. The product indicates this by posting an IntL (Interrupt) signal

with the Data_Not_Ready bit negated in the memory map. Note that on power up (including hot insertion) the module

should post this completion of reset interrupt without requiring a reset.

Initialize Mode (InitMode) is an input signal. It is pulled up to Vcc in the QSFP56 module. The InitMode signal allows the host to define whether the QSFP56 module will initialize under host software control (InitMode asserted High) or module hardware control (InitMode deasserted Low). Under host software control, the module shall remain in Low Power Mode until software enables the transition to High Power Mode, as defined in the QSFP56 Management Interface Specification. Under hardware control (InitMode de-asserted Low), the module may immediately transition to High Power Mode after the management interface is initialized. The host shall not change the state of this signal while the module is present. In legacy QSFP applications, this signal is named LPMode. See SFF-8679 for LPMode signal description.

Module Present (ModPrsL) is a signal local to the host board which, in the absence of a product, is normally pulled up to the host Vcc. When the product is inserted into the connector, it completes the path to ground through a resistor on the host board and asserts the signal. ModPrsL then indicates its present by setting ModPrsL to a “Low” state.

Interrupt (IntL) is an output pin. “Low” indicates a possible operational fault or a status critical to the host system. The host identifies the source of the interrupt using the 2-wire serial interface. The IntL pin is an open collector output and must be pulled to the Host Vcc voltage on the Host board.

Absolute Maximum Ratings

Table1-Absolute Maximum Ratings

Parameter	Symbol	Min	Typical	Max	Unit	Notes
Storage Temperature	TSTG	-40		85	ºC	
Operating Relative Humidity (non-condensing)	RH	+5		85	%	1
Supply Voltage	V_{CC}	-0.5		3.6	V	
Receiver Damage Threshold per Lane	P_{RDMG}	5			dBm	

Notes:

[1] No condensation

Recommended Operating Conditions

Table2-Recommended Operating Conditions

Parameter	Symbol	Min	Typical	Max	Unit	Notes
Case temperature	Tc	0		70	℃	
Supply Voltage	V_{CC}	3.135	3.3	3.465	V	
Power Dissipation	Pd			6	W	
Data Rate				212.5	Gbps	
Link Distance	D			100	m	1

Notes:

[1] OM4 fiber, 70m for OM3 fiber, with KP4 FEC

Electrical Characteristic

The following electrical characteristics are defined over the Recommended Operating Environment unless

otherwise specified.

Table3-Electrical Characteristic

Parameter	Symbol	Units	Min	Typical	Max	Notes
Transmitter						
Signaling rate (each lane)	SR	GBPS	26.5625 ± 100 ppm			
Differential data input voltage per lane	Vin,pp,diff	mV	900			
Differential termination mismatchal	-	%	-	-	10	
Single-ended voltage tolerance range	-	V	-0.4	-	3.3	
DC common mode voltage	-	mV	-350	-	2850	
Receiver						
Signaling rate (each lane)	SR	GBd	26.5625 ± 100 ppm			
Differential output voltage	-	mV	-	-	900	
Near-end ESMW (Eye symmetry mask width)	-	UI	0.265	-	-	
Near-end Eye height, differential (min)	-	mV	70	-	-	
Far-end ESMW (Eye symmetry mask width)	-	UI	0.2	-	-	
Far-end Eye height, differential (min)	-	mV	30	-	-	
Differential termination mismatch	-	%		-	10	
Transition time (min, 20% to 80%)	-	ps	9.5	-	-	
DC common mode voltage	-	mV	-350	-	2850	

Optical Characteristics

Table4-Optical Characteristics

Parameter	Symbol	Units	Min	Typical	Max	Notes
Transmitter						
Signaling rate (each lane)	SR	GBd	26.5625 ± 100 ppm			
Modulation format	-	-	PAM4			
Lane wavelength	λ	nm	840	850	860	
RMS spectral width	Δλ	nm	-	-	0.6	
Average launch power, each lane	-	dBm	-6.5	-	4	
Outer Optical Modulation Amplitude (OMAouter), each lane	-	dBm	-4.5	-	3	1
Launch power in OMAouter minus TDECQ, each lane	-	dBm	-5.9	-	-	
Transmitter and dispersion eye closure for PAM4 (TDECQ), each lane	-	dB	-	-	4.5	
Average launch power of OFF transmitter, each lane	-	dBm	-	-	-30	
Extinction ratio	-	dB	3	-	-	
Transmitter transition time, each lane	-	ps	-	-	34	
Optical return loss tolerance	-	dB	-	-	12	

Receiver

Signaling rate (each lane)	SR	GBd	26.5625 ± 100 ppm			
Modulation format	-	-	PAM4			
Lane wavelength	λ	nm	840	850	860	
Damage threshold, each lane	P_{IN}	dBm	5	-	-	
Average receive power, each lane	-	dBm	-6.5	-	4	
Receive power (OMAouter), each lane	-	dBm	-	-	3	
Receiver sensitivity (OMAouter), each lane	-	dBm	-	-	Max(6.5,SEC Q-7.9)	2
LOS Assert	-	dBm	-30	-	-10	
LOS De-Assert	-	dBm	-	-	-9	
LOS Hysteresis	-	dB	0.5	-	-	

Notes:

[1] Even if the TDECQ < 1.4 dB, the OMAouter (min) must exceed this value.

[2] Bit Error Ratio < 2.4x10-4, Pattern PRBS31Q

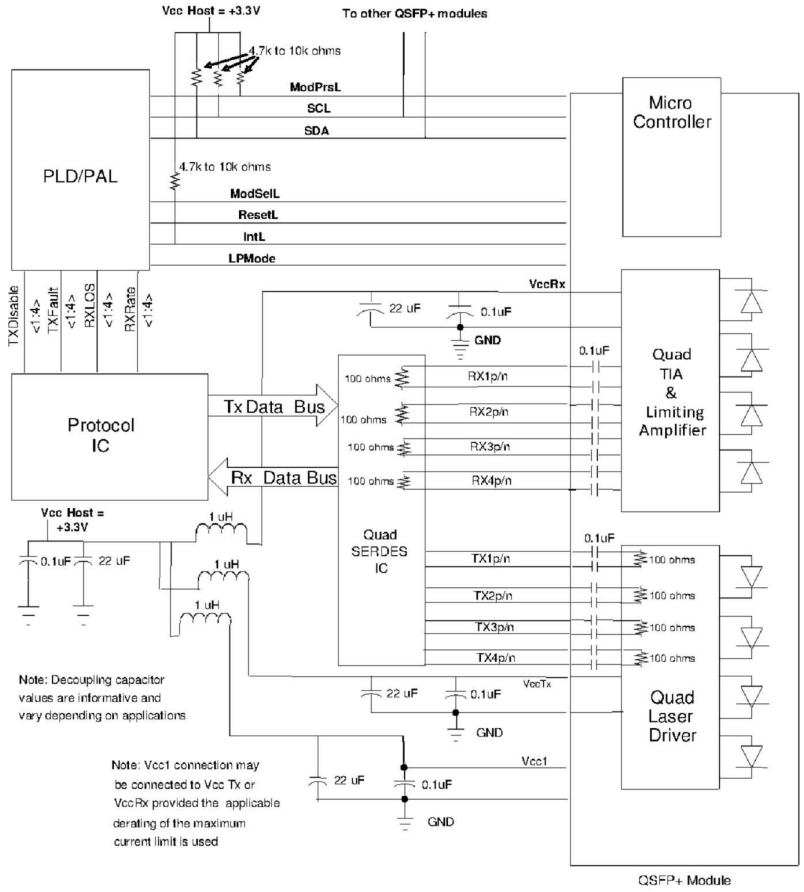


Figure1 Recommended Interface Circuit

Pin Assignment and Description

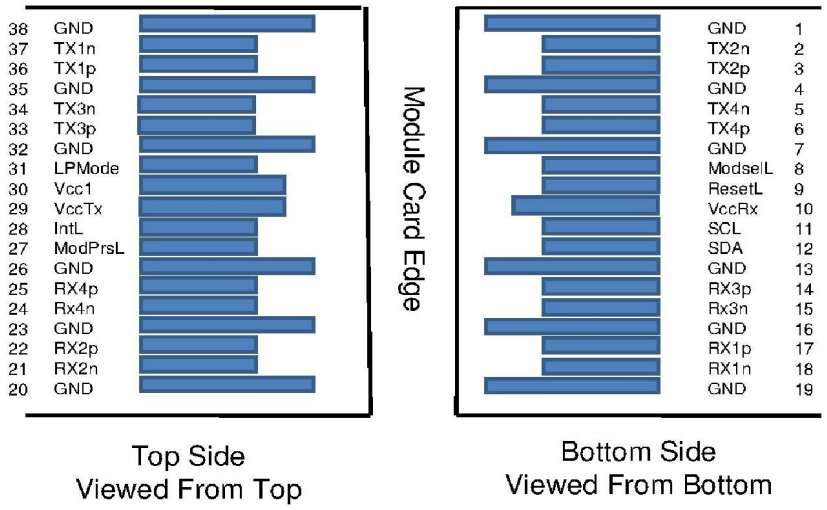


Figure2 MSA Compliant Connector

Table5-Pin Function Definitions

Pin	Symbol	Description	Notes
1	GND	Ground	1
2	Tx2n	Transmitter Inverted Data Input	
3	Tx2p	Transmitter Non-Inverted Data Input	
4	GND	Ground	1
5	Tx4n	Transmitter Inverted Data Input	
6	Tx4p	Transmitter Non-Inverted Data Input	
7	GND	Ground	1
8	ModSelL	Module Select	
9	ResetL	Module Reset	
10	Vcc Rx	+3.3V Power Supply Receiver	
11	SCL	2-wire serial interface clock	
12	SDA	2-wire serial interface data	
13	GND	Ground	1
14	Rx3p	Receiver Non-Inverted Data Output	
15	Rx3n	Receiver Inverted Data Output	
16	GND	Ground	1
17	Rx1p	Receiver Non-Inverted Data Output	
18	Rx1n	Receiver Inverted Data Output	
19	GND	Ground	1
20	GND	Ground	1
21	Rx2n	Receiver Inverted Data Output	

22	Rx2p	Receiver Non-Inverted Data Output	

23	GND	Ground	1
24	Rx4n	Receiver Inverted Data Output	
25	Rx4p	Receiver Non-Inverted Data Output	
26	GND	Ground	1
27	ModPrsL	Module Present	
28	IntL/RxLOSL	Interrupt. Optionally configurable as RxLOSL via the management interface (SFF-8636)	
29	VccTx	+3.3V Power supply transmitter	
30	Vcc1	+3.3V Power supply	
31	InitMode	Initialization mode; In legacy QSFP applications, the InitMode pad is called LPMODE	
32	GND	Ground	1
33	Tx3p	Transmitter Non-Inverted Data Input	
34	Tx3n	Transmitter Inverted Data Input	
35	GND	Ground	1
36	Tx1p	Transmitter Non-Inverted Data Input	
37	Tx1n	Transmitter Inverted Data Input	
38	GND	Ground	1

Notes:

[1] Circuit ground is internally isolated from chassis ground.

Memory Map

Compatible with CMIS rev 4.0.

Optical interface arrangement

The optical port is a male MPO connector receptacle, with fiber lane assignments as shown in Figure 3.

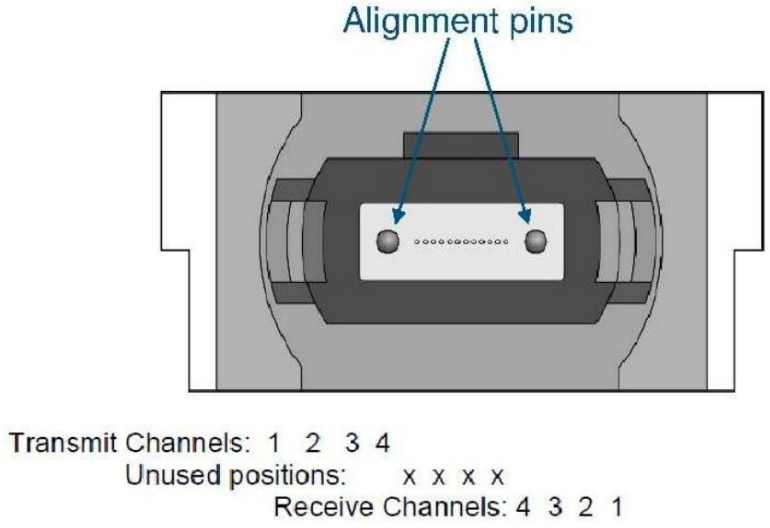
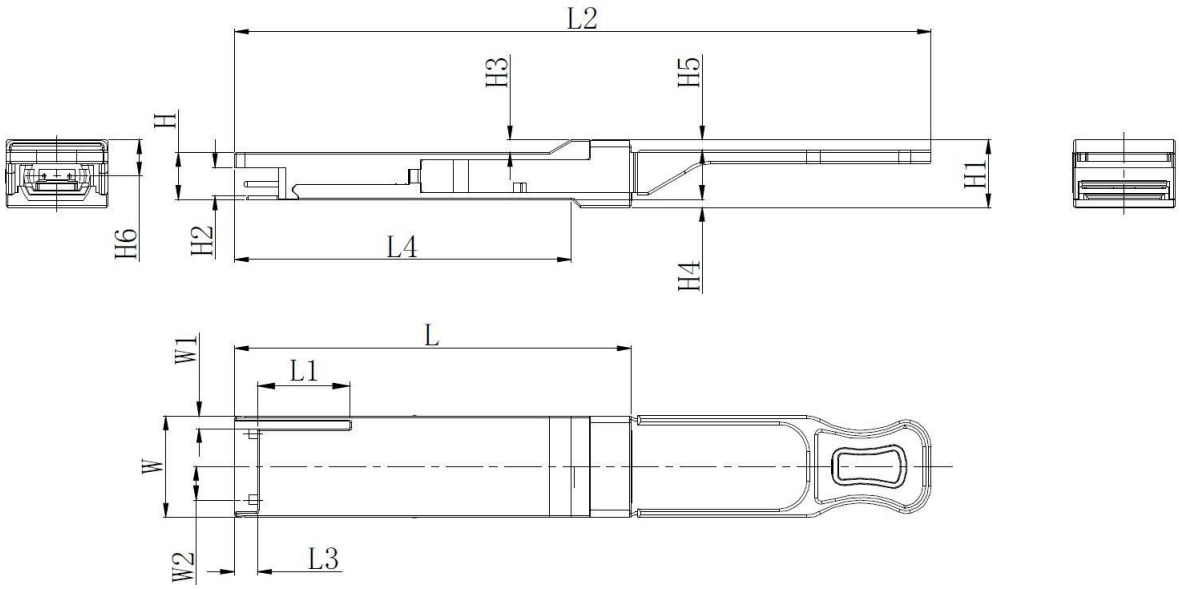


Figure3 Optical interface arrangement

Mechanical



Unit mm

	L	L1	L2	L3	L4	W	W1	W2	H	H1	H2	H3	H4	H5	H6
Max	72.2	-	128	4.35	61.4	18.45	-	6.2	8.6	12.4	5.35	2.5	1.6	2.0	-
Type	72.0	-	-	4.20	61.2	18.35	-	-	8.5	12.2	5.2	2.3	1.5	1.8	6.55
Min	68.8	16.5	124	4.05	61.0	18.25	2.2	5.8	8.4	12.0	5.05	2.1	1.3	1.6	-